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Confirmatory License

Application For: Polyphase Channelization System

Inventor(s): Rajendra Kumar, Tien M. Nguyen

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Contractor: The Aerospace Corporation

By: _____
Gordon J. Louttit
Senior Vice President, General Counsel and Secretary

Business Address: P.O. Box 92957, M1/040
Los Angeles, CA 90009

INVENTION DISCLOSURE

IN DISCLOSING THE INVENTION

1. Discuss the problem which the invention is designed to solve, referring to any similar devices.
2. State the advantages of the invention over devices presently known.
3. Describe the invention and its operation. If necessary, attach signed, witnessed and dated prints, etc.
4. List the features of the invention that are believed to be novel.
5. Have you publicly disclosed this invention? If yes, when? A valid patent cannot be obtained if the invention was publicly disclosed for more than one year prior to the filing of a patent application.
6. Describe potential markets for this patent.
7. Send this disclosure to the Corporate Law Directorate.

Polyphase /FFT Channelizer Architecture based on Parallel A/D Converter

1. Problem Statement: The present and future generations of satellites need to operate with small earth terminals as with mobile vehicle or hand held terminals. Such satellites need to be "user oriented" in that the user terminal needs to be relatively less complex and have small power, weight and low cost requirements. Such an arrangement may be achieved at the cost of increasing the complexity of the space borne equipment and the central earth station(s). An example of such a system is where in the uplink uses FDMA techniques with low cost and complexity terminals while the downlink uses TDMA technique to maximize the satellite radiated power without intermodulation noise. In such systems the small earth terminals do not need the capability of transmitting at very high burst rate and stringent satellite frame synchronization capabilities necessary for TDMA transmitter. The feasibility of mixed mode multiple accessing techniques requires efficient means of translation between the two formats of MA techniques. Although analog techniques are in principle straightforward, in terms of implementation considerations of size, weight, cost and flexibility, direct digital techniques are expected to perform much better. Digital techniques can also fully exploit advances in VLSI and ASIC technologies to achieve these objectives. There are several techniques available for translation (and channelization), namely, analytical signal approach, polyphase/Discrete Fourier Transform (DFT) approach, frequency domain filtering (or FFT filtering) approach, and tree filter bank (or multistage approach). In terms of broadband satellites (bandwidth in GHz(s)), major limitation is in terms of analog to digital (A/D) conversion of the received broadband signal. Such an A/D converter needs to operate at least at a rate equal to two times the received signal bandwidth. This imposes serious limitations in terms of availability of A/D converters operating at such high speeds and/or their high power requirement and cost. In such a situation an analog filter bank may be required to first split the signal into several signals of smaller bandwidth and digitally process each individual signal. Such a hybrid structure suffers from the disadvantages of the analog scheme in terms of weight and power requirements of the analog filters and lacks the advantages of completely digital schemes.

2. Advantages of the Present Invention: This invention deals with the problem of digital signal processing of broadband signals. Broadband signals require A/D converters operating at very high rate imposing limitations in terms of their availability and power requirements. This invention presents a parallel architecture where in several A/D converters of much lower speed operate in synergy to effectively provide a high-speed A/D converter. For example, 10 A/D converters operating at 200 MHz each can be combined to provide a 2 GHz converter. Since A/D conversion is a major bottleneck in extending DSP applications to higher and higher bandwidth signals, this invention eliminates such a restriction in principle, while reduces it by order of magnitude. A specific application of this parallel architecture to polyphase/FFT translator/channelizer is presented.

3. Description of the Invention: Figure 1 shows the proposed parallel architecture of the high speed A/D converter. As shown in the figure, the input broadband signal is routed to a set of N parallel sampling circuits whose sampling instances are provided by polyphase clocks CK_1, Ck_2,...,CK_N . These polyphase clock signals are depicted in Figure 2, illustrated for the case of N=4. In Figure 2, T_H denotes the period of the high rate sampling clock and T_{HS} denotes (for notational purpose only) the sampling time required by the sampler. In actual implementation, sampler and A/D converter may be on a single chip and there such a distinction may not be necessary. In this case the ratio (T_{HS}/T_H) simply denotes the duty cycle of the clock.. In the high rate A/D conversion, the available analog to digital conversion time is T_H-T_{HS}. Note that $T_{HS} << T_H$ as the sampling operation merely involves switching of an analog gate and charging a capacitor through this gate after which the capacitor holds the sample value during the A/D conversion process which involves sequential processing. In the proposed parallel architecture, the available time for sampling is $T_{LS} = T_H$ with T_L-T_H time available for A/D conversion where $T_L = NT_H$ is the total time available for sampling and A/D conversion. As mentioned earlier, sampling is a fast process and can be performed in period T_H ($T_H >> T_{HS}$). However, more important is the fact that the A/D conversion time is now extended to T_L-T_H = (N-1)T_H. Thus by simply increasing the value of N, this period can be enlarged to any reasonably desired value. The buffers in Figure 1 hold the binary word representing the sampled value for T_L sec duration. At the end of this interval, the digital multiplexer reads out the buffer to the output during the interval determined by the corresponding clock CK_i, i=1,2,...,N. Since the digital multiplexer merely involves digital gating operation, it can operate at high speeds without limiting the speed of operation of the overall circuit. In fact in many applications, it may be required to split the digital signal in to M streams using a digital demultiplexer. In such cases, both multiplexer and demultiplexer are eliminated when N is selected to M and considerably simplified when N is selected not equal to M. One such application involves digital channelizer described in the following.

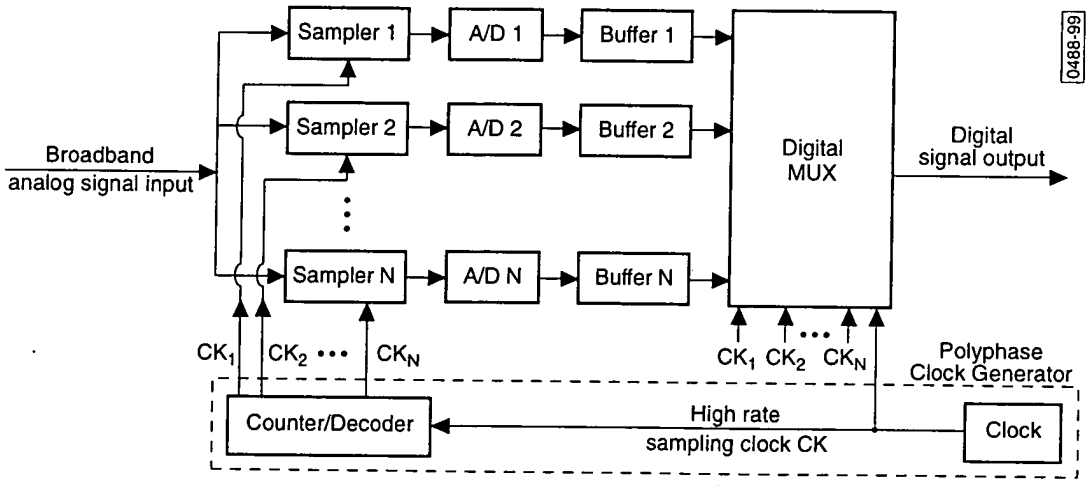

Figure 1. Parallel architecture of A/D converter.

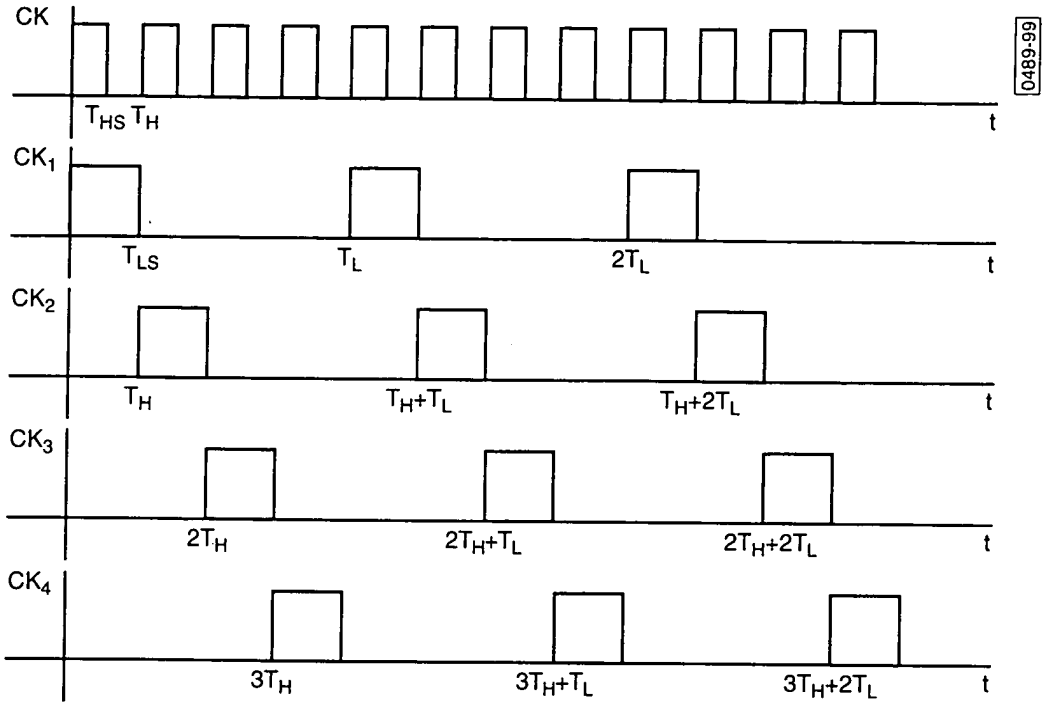

Figure 2. Timing diagram of polyphase clocks.

Figure 3 shows such a channelizer when integrated with the parallel A/D converter architecture. In the proposed channelizer scheme, the received wideband r.f. signal after being amplified by LNA (low noise amplifier) filtered by r.f. bandpass filter, and possibly down converted (optional) to an intermediate frequency f_{IF1} is input to the integrated polyphase/FFT channelizer of Figure 3. In this unit, the signal is input to a complex mixer whose output is an analytic complex-valued bandpass signal at selected IF frequency f_{IF} and bandwidth B_{IF}. The complex-valued signals are shown by double lines in Figure 3. This analytic signal when down sampled at a rate $f_{SH} = 1/T_{SH}$ higher than $2B_{IF}$ and equal to an integer sub multiple of f_{IF}, and A/D converted will yield the desired complex-valued baseband signal in digital form. Such baseband signal is then demultiplexed in to M channels which are individually filtered by digital polyphase filters with impulse responses u_1 (m),u_2(m),...,u_M(m) respectively. Integrating this procedure with the parallel A/D converter architecture of Figure 1 results in the architecture of Figure 3. In Figure 3, The IF signal is input to M low rate A/D converters whose outputs are input to the respective polyphase (operating at low rate) digital filters. The outputs of the polyphase filters are processed by the FFT processor, which involves computation of FFT transform along with some auxiliary arithmetic operations depending upon the detailed design of the polyphase scheme. The output of the FFT processor are the desired complex baseband signal whose real and imaginary parts are the desired baseband channel signals. Note that this architecture altogether eliminates any high rate digital signals, except that the sampling duration allowed for the samplers must be smaller than T_H as explained earlier with reference to Figures 1-2.

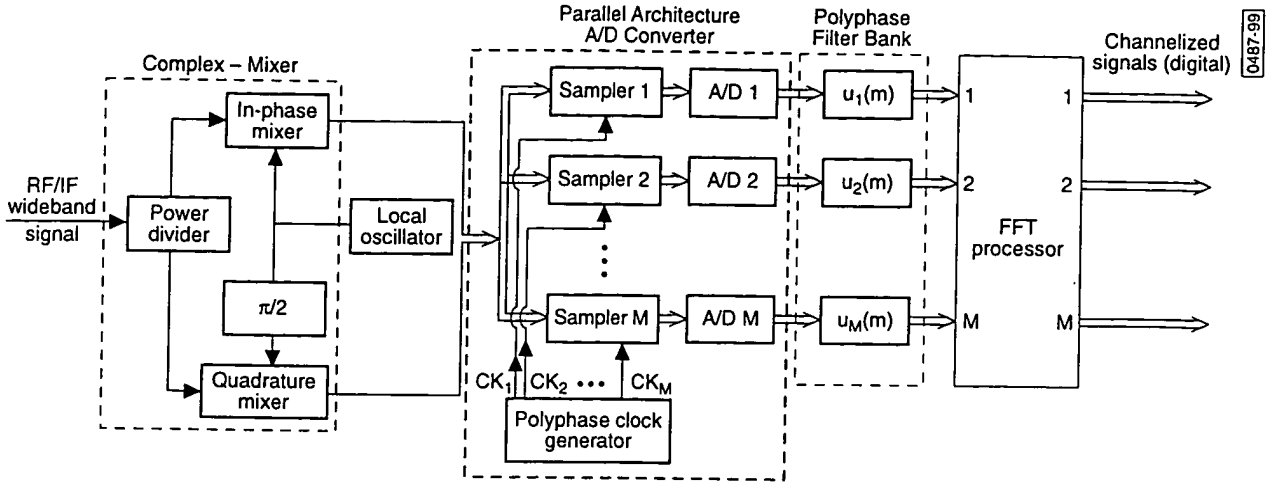

Figure 3. Novel Polyphase/FFT channelizer.

4. Novel Features of the Invention:

1. A novel parallel architecture of low speed A/D converters to create a high speed A/D converter.
2. Increases the frequency range over which A/D conversion can be performed by orders of magnitude.
3. The configuration is simple and modular. Can be incorporated in a chip set or a single VLSI/ASIC chip.
4. Can be integrated with Polyphase/FFT architecture providing very efficient translator/channelizer for wideband signals.

5. The invention has not been publicly disclosed.

6. Potential markets of the invention:
The invention should have broad market covering fields of DSP and Communications especially involving broadband signals where the A/D conversion may be a bottleneck.

PLEASE WRITE SIGNATURES AND DATES IN BLACK INK

INVENTOR	DATE	INVENTOR	DATE	INVENTOR	DATE
Rajendra Kumar	5/11/99	Tien M. Nguyen	5/11/99		
ORGANIZATION AND CCC		ORGANIZATION AND CCC		ORGANIZATION AND CCC	
Electronic Systems Division 5232		Electronic Systems Division 5232			
WITNESSED, READ AND UNDERSTOOD BY:		DATE: 5/11/99	AND BY:		DATE: 5-11-99